

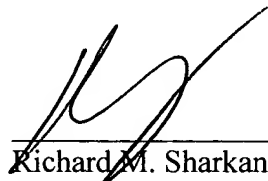
Attorney Docket No. 00P7925US (IFX-060PUS)

Application No. 09/669,585

Filing Date: September 26, 2000

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-0845.

Respectfully submitted,



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Attachment: Sheet showing changes made
IFX-060PUS -Response to Office Action dated 051702

CLAIM COMPARISON

2. (Amended) A memory cell comprising:
- a trench capacitor formed in a substrate;
 - a shallow transistor trench (STT) formed in the substrate;
 - a transistor comprising:
 - a first diffusion region, the first diffusion region couples the ~~transistor~~ capacitor to ~~the~~ a gate of the transistor;
 - a second diffusion region, the second diffusion region couples the transistor to a bit line; ~~and~~;
 - wherein the a gate serving serves as a word line;
 - wherein the gate includes a buried portion and a non-buried portion, wherein the buried portion of the gate occupies the shallow transistor trench; and
 - wherein the buried portion of the gate is in contact with the first diffusion region.
5. (Amended) The memory cell of claim 3 wherein the first diffusion region is located in a region of the substrate between the trench capacitor and STT and an interface of STT and the substrate between the first and second diffusion ~~region~~ regions forms a channel of the transistor.
- 10 (Amended) The memory cell of claim 9 wherein the gate further comprises a cap layer over the non-buried portion of the gate.
12. (Amended) The memory cell of claim 11 wherein the gate further comprises a cap layer over the non-buried portion of the gate.